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Stability of Interfaces in Gold-Silicon System Regarding Equilibrium Segregation

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Abstract. — The Si/Au system has been intensively studied for its application in the field of microelectronics. This paper presents results obtained on segregation and interaction phenomena in such a system for a range of temperature below the eutectic (363 °C). Investigations were performed using two complementary techniques: Auger Electron Spectroscopy (AES) and Transmission Electron Microscopy (TEM). The importance of the microstructure on the segregation phenomenon is shown. Indeed, the driving force of the gold/poly-silicon system evolution is silicon recrystallization followed by superficial silicon segregation on silicon-gold mixture even at very low temperatures.

Résumé. — Le système Si/Au a été largement étudié à cause de ses applications dans le domaine de la microélectronique. Dans ce papier, nous rapportons sur ce système des résultats relatifs aux phénomènes d'interaction et de ségrégation à des températures inférieures à celle de l'eutectique (363 °C). Deux techniques complémentaires d'investigation ont été utilisées: la Spectroscopie d'Électrons Auger (SEA) et la Microscopie Électronique en Transmission (MET). Nous montrons que la microstructure influence fortement le phénomène de ségrégation : la force motrice de l'évolution du système or/silicium polycristallin est la recristallisation du silicium suivie par la ségrégation superficielle de ce dernier sur le mélange silicium-or ainsi formé, à très basse température.

Introduction

The interactions between gold and silicon have attracted a great deal of attention largely motivated by the extremely low eutectic temperature (363 °C). It was noticed quite early that the oxidation of silicon occurs at a very low temperature in the presence of gold [1]; this is to be compared to detailed surface observations of the interactions between oxygen and silicon with fractional monolayers of gold [2]. Although equilibrium compounds do not exist, metastable gold-silicon compounds have been prepared [3, 4]. Curious morphological instabilities have

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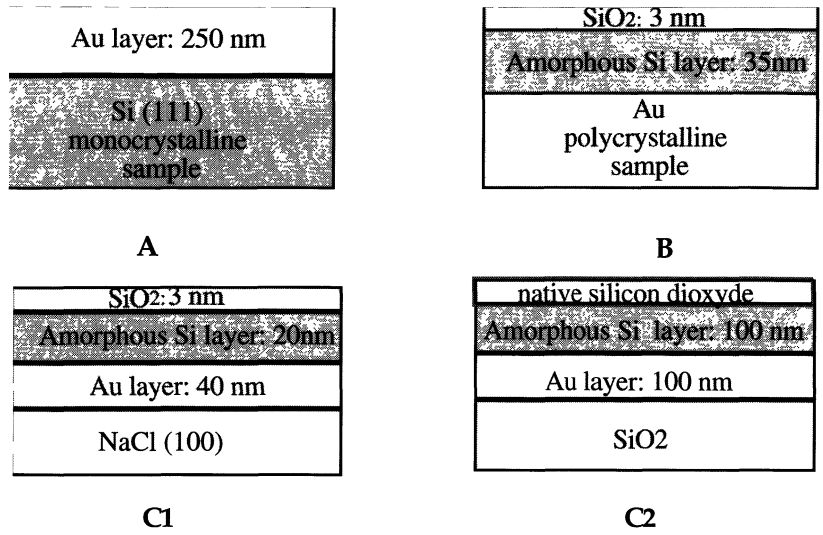


Fig. 1. — Configuration of the as-prepared bilayers.

been observed in bilayers of polycrystalline silicon and gold: upon heat treatment the physical order of the bilayers becomes inverted [5]. The reason for such a phenomenon, which occurs whenever polycrystalline silicon (deposited at low temperature) is in contact with another material with sufficiently high diffusivity, is the grain growth of the polysilicon [5, 6]. The second material provides the medium through which silicon is mobile (necessary for growth) at temperatures much below those at which silicon mobility is observed in pure silicon. With respect to the already mentioned low eutectic temperature, strong interactions exist between the two elements in the liquid state (negative enthalpy of mixing), leading to short range order (negative entropy). In the absence of equilibrium solid state compounds, stability of the liquid solution is enhanced [7]. Small amounts of gold are known to increase the rate of epitaxial growth of amorphous silicon on monocrystalline substrates (solid state epitaxy) [8].

1. Objective

The present experiments were undertaken with the purpose of shedding some light on the importance of the stability of the microstructures on the surface segregation phenomena observed for temperatures lower than the eutectic one in gold-silicon system. Investigations were performed using two complementary techniques: AES and TEM (plane and cross-section view). The first one provides profiles as a function of heat treatment duration whereas the second technique gives information about the structure and the microstructure of the film.

2. Experimental Procedure

Three sets of samples were prepared, namely, (A) thin layer of gold deposited *via* evaporation on monocrystalline silicon substrates, (B) amorphous Si layer on Au polycrystalline samples and (C) bilayers of amorphous silicon and gold deposited in this order onto NaCl (100) substrate (C1) or SiO2 (thermally oxidized silicon wafers C2). Configuration of the as-prepared layers is shown in Figure 1.

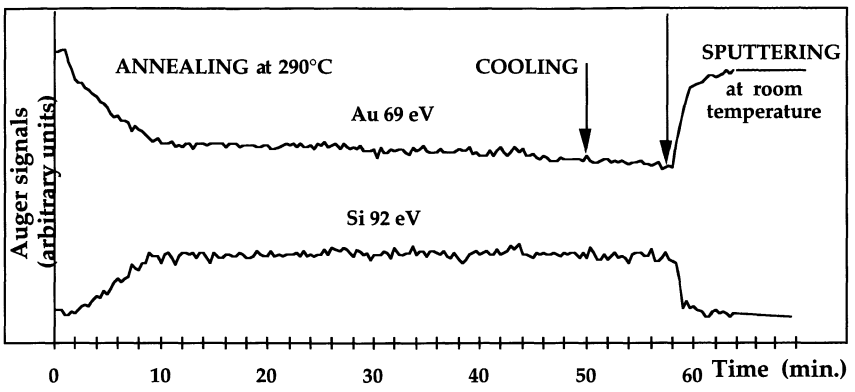


Fig. 2. — Evolution of the Auger signals of both Si (LVV peak at 92 eV) and gold (NVV peak at 69 eV during annealing of the sample A at 290 °C and, after cooling, during sputtering of the surface.

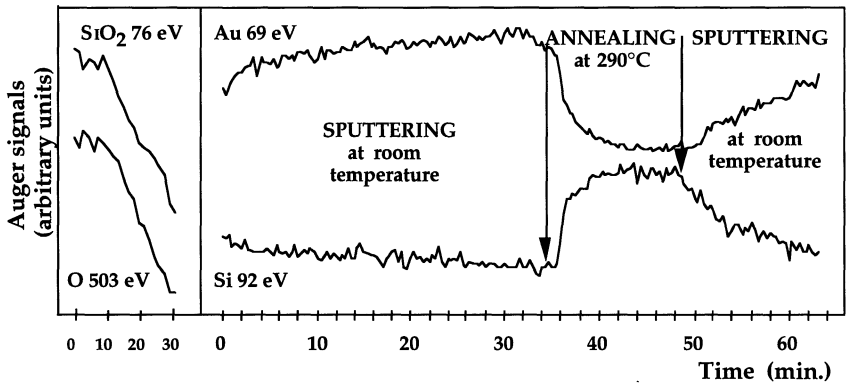


Fig. 3. — Evolution of the Auger signals of both Si (LVV peak at 92 eV) and gold (NVV peak at 69 eV) during sputtering of the surface after annealing of the sample C at 290 °C.

AES studies are performed in a conventional UHV chamber equipped with a LEED optics and with a cylindrical mirror analyser (RIBER). Auger spectra were recorded in differential mode. The samples are cleaned *in situ* by argon ion bombardment. Argon ion etching conditions are the following: ion energy = 2 keV, Ar base pressure: 5×10^{-3} Pa, sputtering rate: 0.1 nm/min. The layers (A, B and C1 type) were heated at 290 °C with an intensity-regulated DC power supply. The chosen temperature as measured by a chromel/alumel thermocouple set on the surface is held for 2 min and is kept constant (±2 °C) during annealing. The peak-to-peak height variations as a function of time were monitored using a computer-controlled system. The transitions used for data analysis are respectively Si (LVV) at 92 eV and Au (NVV) at 69 eV.

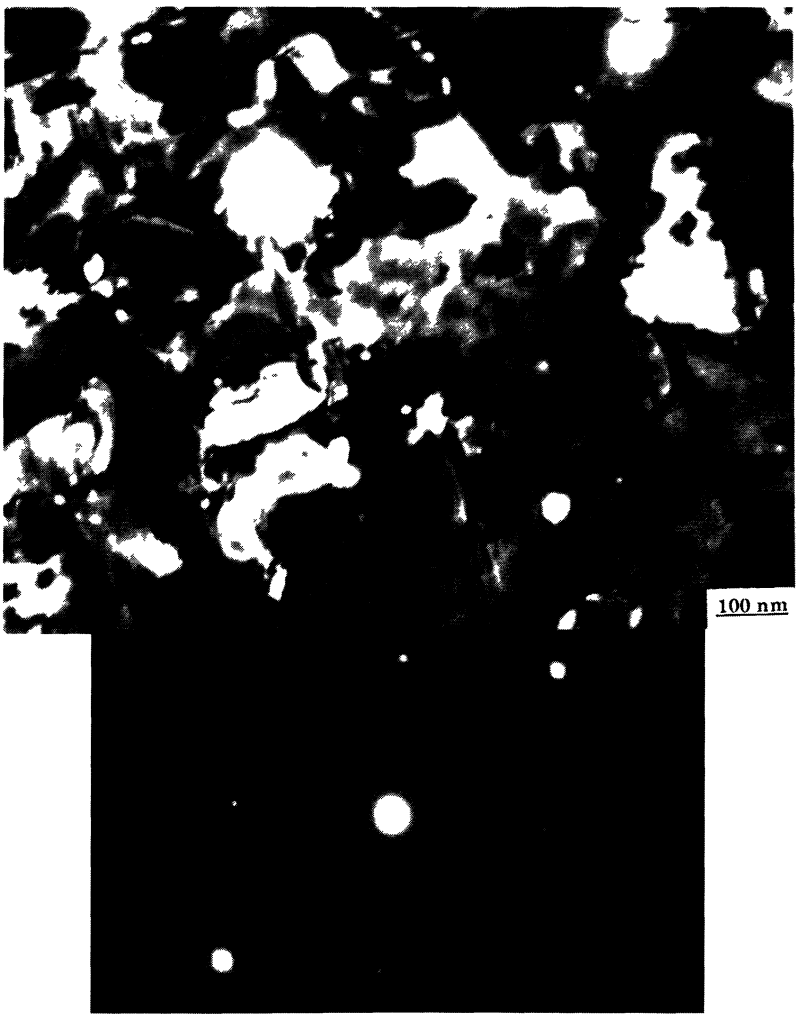
TEM observations were performed on a Philips EM 400 T microscope operating at 100 kV; bright field, dark field, diffraction and convergent beam diffraction were used in this study. Plane view (C1 type sample) and cross-section (C2 type sample) observations were conducted on the as-deposited layer as well as on the layer annealed at 290 °C for 20 h in UHV.

3. Results and Discussion

3.1. Auger Analysis

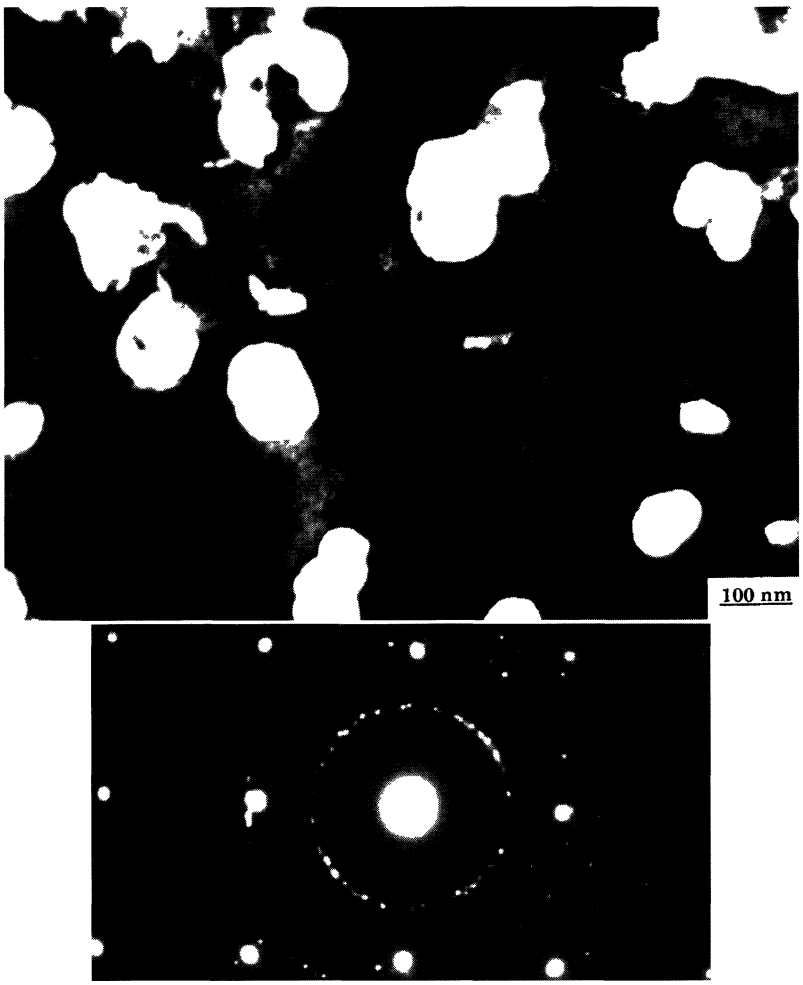
Two cases can be distinguished depending on whether the silicon is a single crystal or not.

In Figure 2, the variations of Auger signals of Au and Si are plotted *versus* time for sample (A). One can see that in the first stage of the annealing at 290 °C, the Si signal is increasing while the Au one is decreasing. After 10 minutes both signals reach a constant value which corresponds to the maximum Si coverage. To quantify this Si amount, annealing is stopped. Then, the segregated Si is removed by sputtering at room temperature: after 3 minutes a spectrum characteristic of gold is obtained. Note that a new annealing of this sample in the same conditions as above leads to Si surface segregation. The segregated silicon quantity is evaluated to about one monolayer using a calibration done on the Au signal attenuation [9].



a)

Fig. 4. — Micrograph (plane view) and the corresponding diffraction of (sample C1): a) the as-deposited bilayer, b) the bilayer after annealing at 290 °C during 20 h in UHV.



b)

Fig. 4. — *(Continued)*

In view of such an experimental protocol, this can be regarded as superficial equilibrium segregation of silicon. This is observed when a gold layer is deposited on a silicon single crystal. This segregation can be easily related to the relative surface tensions of Au and Si, 1 138 mJ/m^2 and 735 mJ/m^2 respectively [10].

When a silicon layer is deposited onto gold surfaces (sample B, C1 or C2), AES analysis indicates the existence of a superficial non stoichiometric oxide on the silicon layer. The evolution of the bilayer *versus* temperature depends on whether this superficial oxide layer is removed or not. In the first case, a superficial contamination by carbon is observed even in UHV; this contamination is due to the high reactivity of the deposited silicon and hides any other phenomenon. However, in the second case, only a substantial decrease of the silicon signal is observed when the bilayer is annealed during 24 h at 290 °C. After this annealing, sputtering of the sample was performed at room temperature to determine the in-depth distribution of Au and Si in the bilayer. The variations of the Auger signals are plotted *versus* time (Fig. 3) following this sequence: ion etching, annealing at 290 °C and new etching. It can be seen

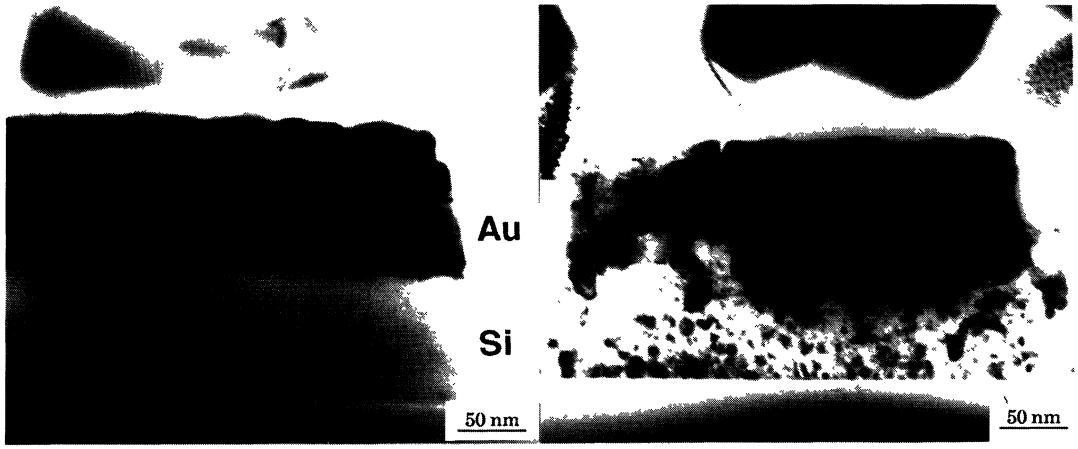


Fig. 5. — Micrograph (cross-sections) (sample C2): a) the as-deposited bilayer, b) the bilayer after annealing at 290 °C during 20 h in UHV.

that the superficial oxide layer is first removed; then, the spectrum exhibits only a high signal corresponding to Au and a small one corresponding to Si: the layer underneath the oxide is a silicon-gold mixture rich in gold. Moreover, when the sputtering time increases, the Au signal increases while the silicon one decreases. When this mixture is stabilized, annealing of the sample at 290 °C leads to silicon equilibrium surface segregation on the uppermost layer as observed for sample (A).

To summarize these AES investigations, superficial segregation of silicon is evidenced in any case. However, for gold/poly-silicon bilayer this phenomenon is only observed after stabilization of this system *i.e.* either formation of gold silicide or microstructure evolution which is not detected by AES. To settle this question we have investigated the same sample by TEM.

3.2. TEM Observations

The micrograph and the corresponding diffraction of the as-deposited C1 bilayer and after heat treatment at 290 °C during 20 h are shown in Figure 4. The observation of the as-deposited silicon on gold shows that the silicon is amorphous and the gold can be either monocrystalline or polycrystalline (see Fig. 4a). After annealing under UHV, crystallization of silicon is observed giving rise to large and isolated Si particles on the gold surface. No evidence of formation of crystalline silicide was observed (Fig. 4b).

To fully understand this last result, cross-section views are performed on sample C2 as shown in Figure 5. The interface between gold and silicon in the as-deposited layer is well defined (Fig. 5a). Annealing of the sample allows crystallization of the silicon but the physical order in the bilayer is almost inverted. The mobility of silicon in the gold layer, most likely *via* the grain boundaries as revealed by TEM observations (Fig. 5b), is high enough to induce silicon crystallization.

4. Conclusion

The use of two complementary techniques such as AES and TEM allows us to get interesting information on the stability of interfaces in gold-silicon system regarding equilibrium segregation.

The main results of this work are the following.
1) Superficial equilibrium segregation of silicon on gold surface is observed at temperatures below the eutectic in the gold/silicon system. This phenomenon is observed only when the microstructure of the bilayer is stable. In the case of the deposited silicon (amorphous), its crystallization begins at very low temperatures.
2) The presence of gold plays a beneficial role for this crystallization. This is related to the high mobility of silicon in gold. Silicon crystallization occurs after mass transport of silicon in the gold layer *via* the grain boundaries acting as diffusion short-circuits. Thus, if the annealing time is long enough, the physical order of the Au/Si bilayers can be inverted. No evidence of the formation of crystalline silicide is observed.

Two situations can be distinguished: In the case of silicon single crystal, the driving force is the segregation of silicon on the gold surface. In the case of polycrystalline silicon (deposited at low temperature), first there is a system reorganization which includes silicon crystallization at very low temperature after diffusion through the gold layer. Second, after this layers mixing, silicon segregation is observed on the resulting gold-rich phase.

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