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The Role of Auger Electron Spectroscopy in the Semiconductor Industry

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Abstract. — The extremely demanding materials specifications of the electronics industry provides an interesting example of how Auger Electron Spectroscopy is now being put to work to provide valuable input into materials processing and device technology.

1. Introduction

The technique of Auger Electron Spectroscopy (AES) has become widely used in the semiconductor field since its inception in the late 1960's. During this period, semiconductor technology has made enormous advances, and to a large extent the development of AES has paralleled this progress. The circuit complexity and density of modern electronic devices, however, continues unabated as technology extends to smaller dimensions, both laterally and in thickness, with many device structures now reduced to nm dimensions. Assessment techniques are therefore continuously being developed to cope with the changes in technology.

State-of-the-Art AES with primary beam diameters of 50 nm and analysed lateral resolution slightly greater than this due to the back scattering contribution [1-3] is not likely to be greatly improved upon, certainly from a practical point of view. This does not mean that progress in the field has come to a standstill, on the contrary, impressive improvements continue to be made, not only in electron energy analysers [4, 5] and data handling software [6], but in the availability of essential background information such as back scattering and inelastic mean free path corrections [7, 8]. With advanced scanning AES systems [9], it is now possible to simultaneously collect electrons from several Auger peaks, together with other electrons scattered from the sample. Such a multi-spectral/multiple imaging approach provides not only Auger images, but images with chemical and work-function contrast which can be used to analyse surface and sub-surface inhomogeneities.

In common with many other industrial applications of AES, the semiconductor industry relies on the powerful combination of AES and the process of sputter etching to obtain the information it requires. There is a price to pay for this combination, however, by way of the added complication in analysis due to the sputter induced artefacts at the sample surface [10, 11]. The most serious

of these are changes in surface roughness and composition which limit quantitative analysis and achievable depth resolution in Auger depth profiling [12]. The aim of this paper is to give a broad view of the contribution made by AES in the characterisation of semiconductor materials and electronic device structures.

2. Semiconductor Materials

The material that springs most readily to mind when semiconductors are mentioned is silicon. It is still without doubt the most important material in the fabrication of devices and has much to commend it in terms of strength, simple chemistry, uniform sputtering habit, usable natural oxide and general predictable handling characteristic. These qualities are important not only for device fabrication, but are of considerable assistance in its characterisation by the various analytical techniques. The more recent compound materials, however, are very different and something of a challenge for AES. III-V material for example is a term which covers a wide range of binary, ternary and quaternary compounds (Tab. I), each with its own unique set of physical and chemical characteristics. Sputter induced artefacts for example vary enormously across the range of III-V compounds and where sputtering is involved in sample preparation or analysis, it is essential that these effects have been studied in previous experiments if accurate analysis is to be accomplished. In addition to semiconductor materials, a typical device will also contain dielectric regions, metallic contacts and dopants. The range of electronic devices produced by the industry is enormous and likewise, the range of materials used in their fabrication. Rather than itemising these materials, it is more useful to include a table showing the general range of AES applications (Tab. II).

Table I. — *III - V semiconductor compounds used in device structures.*

	Ternary Compounds
	GaInAs
	InGaAs
Binary Compounds	GaInP
GaAs	GaAsP
InAs	AlInAs
InP	
GaP	Quaternary Compounds
	GaInAsP
	GaAlInP
	GaAlInAs

3. Auger Profiling

There are very few investigations carried out by AES that do not involve sputter etching, either to remove surface contamination or in the production of a so called Auger depth profile. This

Table II. — *A review of routine AES applications in the semiconductor industry.*

Surface contamination, usually associated with a process step
End point determination in chemical and ion beam etching process steps
Profiling of thin dielectric layers for stoichiometry and impurities
Profiling of multi-layer metal contacts for interdiffusion
Quantification of matrix elements in semiconductor thin layer structures
Quantification of composition graded compound semiconductors
Quantification of high dose implants in semiconductors
Segregation behaviour of additives in thin metal layers
Thickness measurement of thin films
Thin film adhesion problems
Profiling for contamination at interfaces
Failure analysis of microelectric devices
Wire bonding problems

Table III. — *Sputter etch related phenomena which can degrade AES quantification.*

Atomic mixing	{ Recoil implantation Cascade mixing
Initial condition of sample service	
Non-planar removal of material	
Damage or radiation induced diffusion	
Preferential sputtering	
Surface segregation and migration	
Redisposition of sputtered material	
Surface roughening	

technique, which is a combination of surface analysis and sputtering has given AES a depth dimension and become a powerful tool in determining the depth contribution of composition in thin films [15]. The most common method of producing an Auger profile is to sputter for some pre-determined time period followed by surface analysis. This sequence is repeated for as long as it is necessary to complete the profile. Other methods are available, which are covered in the following section, but if sputtering is involved in the process, complications can arise in the analysis. This is a result of the wide range of sputter induced artefacts that can occur with many materials (Tab. III). There are methods of reducing some of these effects and some are included in this

article. The reader is referred to the literature for a more detailed discussion [16]. An example of how serious sputter related phenomena can be is shown in Figures 1a and 1b. These are secondary electron microscopy (SEM) images of the surface of InP following Ar⁺ sputter etching, and is the combined effect of preferential removal of P and the coalescence of the free In at the surface to form islands of metallic In [17]. This acts as a precursor to the surface roughness that develops with continued sputtering. This effect can be prevented by cooling the sample to liquid N₂ temperatures, not very convenient for general use but fortunately very few materials suffer such gross effects.

4. Bevel Profiling

An alternative method of profiling is the crater-edged profile [18]. This entails sputtering a crater to the required depth in a single stage and performing analysis on the wall of the crater using a small diameter electron beam probe. This has certain advantages, but suffers from the distortions introduced by the “non-linear” crater wall. Ball cratering and angle lapping [20] are other methods of forming bevels. These are prepared by abrasive polishing and are really only suitable for very thick films. Chemical etching to produce a bevelled sample has also been used successfully [21]. A more recent development has been the ‘ion beam bevel section’ [22]. With this method, a finely focused ion beam is rastered in such a way as to sputter a very shallow bevel into the surface of the sample to expose the region of interest. Figure 2 shows how the bevel produces a magnified projection of the buried structure. The bevel angle will be a function of sputtered depth and bevel excursion. Vanishingly small bevel angles are possible on planar surfaces allowing lateral magnification in excess of any practical value (Fig. 3). The linearity of the bevel, which affects the accuracy of the depth scale is limited only by any variations in sputter yield with depth.

The benefits of ion beam bevel sectioning include:

- Any number of elements can be profiled under optimised conditions.
- Unsuspected contaminants may be discovered.
- It allows a high density of data in regions of specific interest.
- The method also has the potential of reducing some of the sputter induced artefacts outlined in Table III.

The first example of how sputter damage can be reduced is shown in Figure 4 and demonstrates the effectiveness of ‘post sputtering’ a bevelled sample. In this instance a sample containing a buried SiO₂ layer has been bevel sectioned using 4 KeV Xe⁺ ions, followed by post sputtering at 1 KeV, resulting in a reduction in the thickness of the atomic mixed region such as to improve the in-depth resolution of the profile by a factor of 2.

An SEM image of a bevel is shown in Figure 5a, the sample in this case is a GaInP/InP superlattice sputtered to a total depth of around 1800 Å. The layers have a period of 220 Å, with each layer nominally the same thickness. A line scan across the bevel with the electron energy analyser locked onto P is shown in Figure 5b and the uniform periodicity is a good demonstration of the bevel’s linearity. Because of the thickness of the layers, however, the problem of preferential sputtering of the P is not apparent, as evidenced by the failure of the line scan to show a constant composition portion at either the top or bottom of a single period. Thicker InP layers are necessary for this effect to become evident.

In Figure 6, the result of bevelling a superlattice sample with thicker InP layers provides an interesting example not only of the P depletion under discussion, but also presents an opportunity

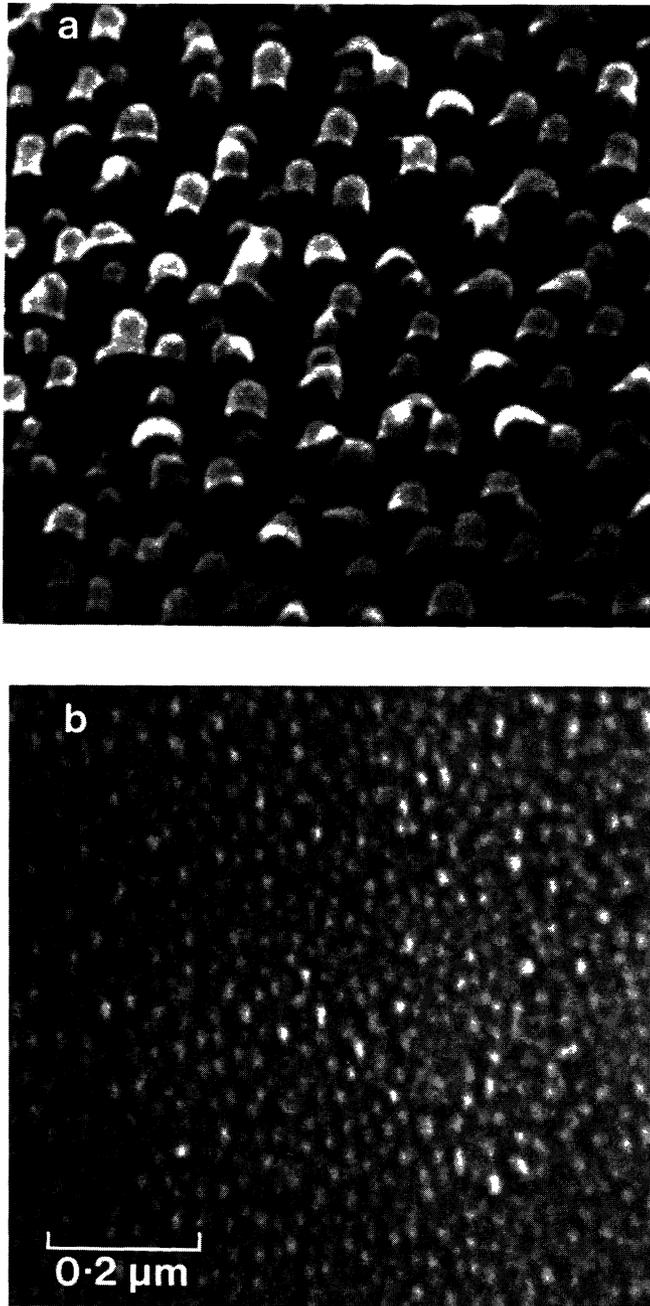


Fig. 1. — SEM micrographs of InP targets after Ar⁺ sputter etch removal of a) 2000 Å and (b) 200 Å.

to describe another method of reducing sputter induced damage. Line scan b) in this figure shows skewing of the In line as a result of P depletion, line scan a) was recorded after post sputter treatment of the bevel using chemically assisted reactive ion beam etching (CARIBE) [23]. With this

Auger Bevel Profile Analysis of a Laser Structure

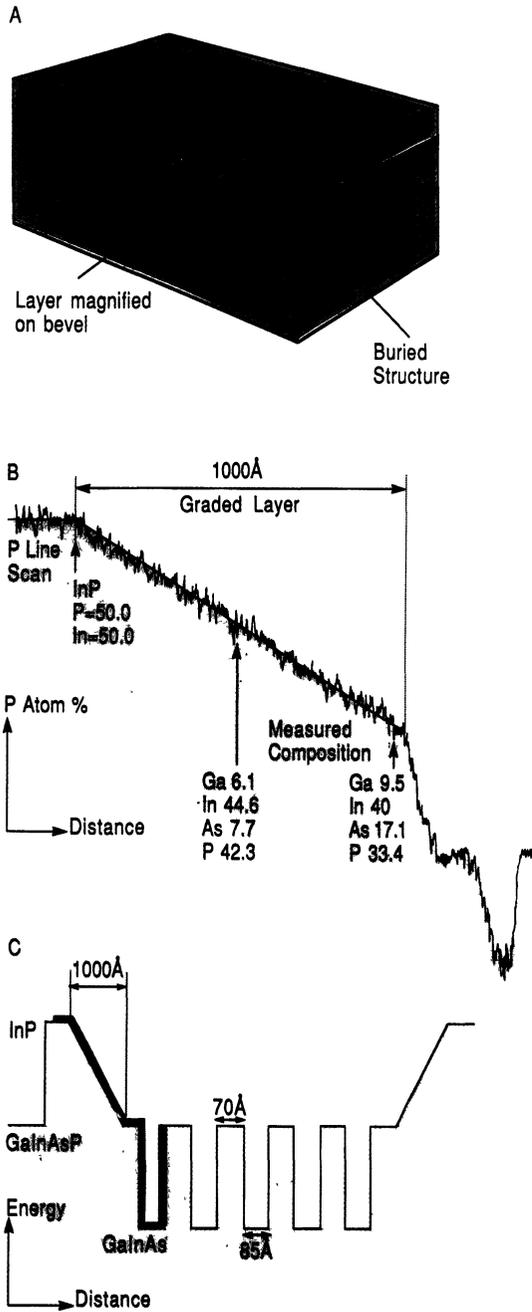


Fig. 2. — a) Schematic of an ion beam bevelled section showing the magnifying effect of the bevel; b) compositional data using Auger line scan from bevelled quaternary laser structures; c) energy level diagrams of quaternary laser structure with bevelled region outlined.

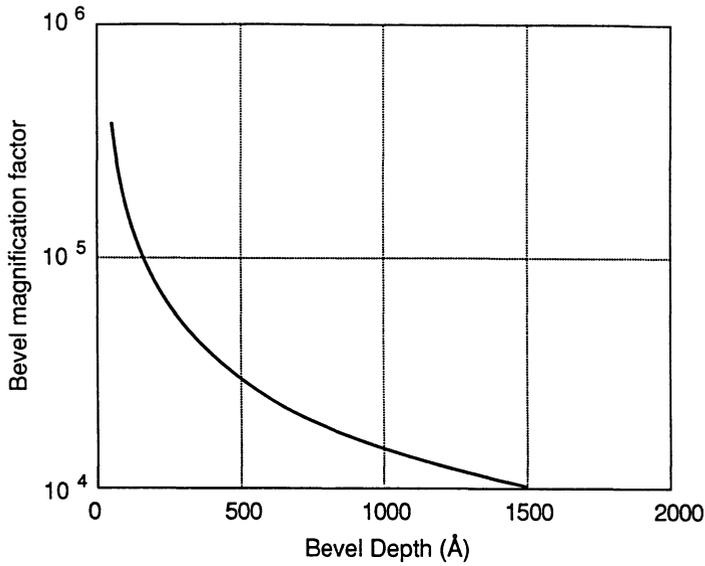


Fig. 3. — Plot showing relationship between depth of bevel and magnification factor for bevel 1.5 mm long.

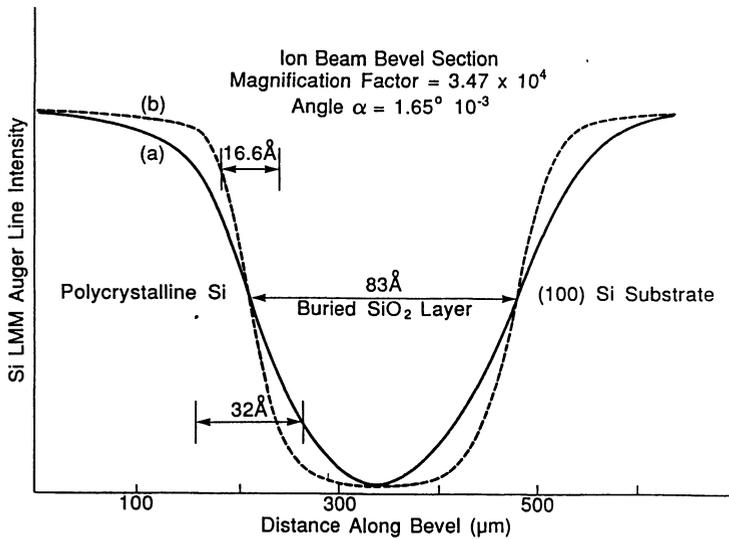


Fig. 4. — Si (92 eV) line scans across ion beam bevelled sectioned buried SiO₂ layer: a) as bevelled using 4 KeV Xe+ ions at normal incidence; b) the same bevel following sputter removal of ~ 100 Å of the surface using 1 KeV Xe+ ions incident at 60° from the normal.

method Ar and O₂ gas ions at low energy are incident upon a sample that sits in a Cl atmosphere.

The method is effective at room temperature and etches by the absorption and chemical reaction of Cl at the same surface which reduces considerably the energy requirement from the incident ion beam to promote sputtering. It is clear from the line scan that this treatment has removed any indication of preferential loss of P. More surprising was the improvement in interface

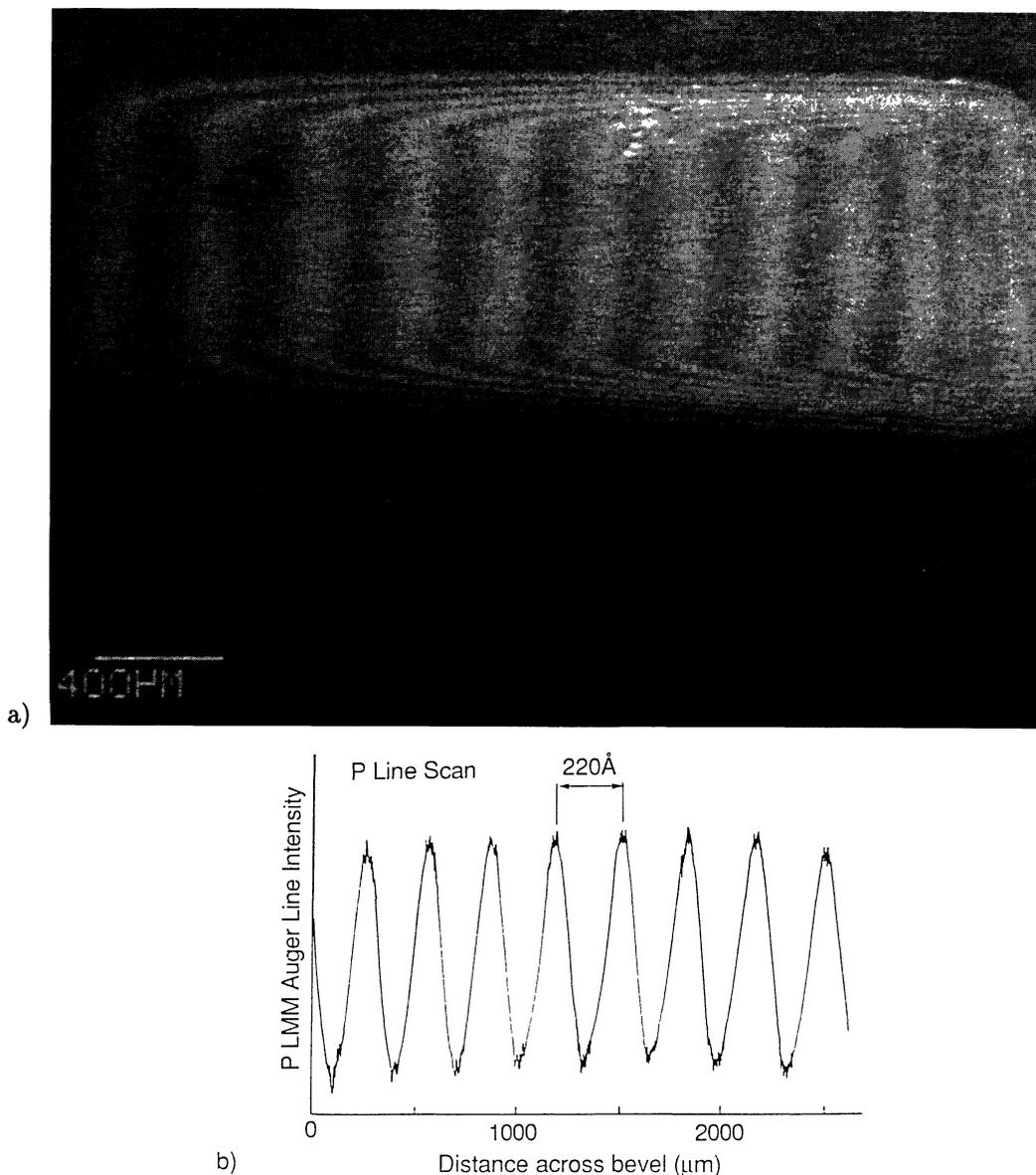


Fig. 5. — SEM image of ion beam bevel section sputtered into a) 220Å period superlattice of GaInAs/InP; b) P line scan across bevelled section covering 90% of bevel length.

resolution of around 50%. This unexpected result suggests that the surface of the bevel, already roughened by its preparation using Xe^+ ions has undergone planarisation. The CARIBE process for this work was carried out external to the AES system for reasons of the required Cl atmosphere.

5. Laser Structure Characterisations

Solid state laser structures (Fig. 7) are very complex affairs and present something of a challenge to the analyst containing, as they do, a range of binary, ternary and quaternary compounds, in

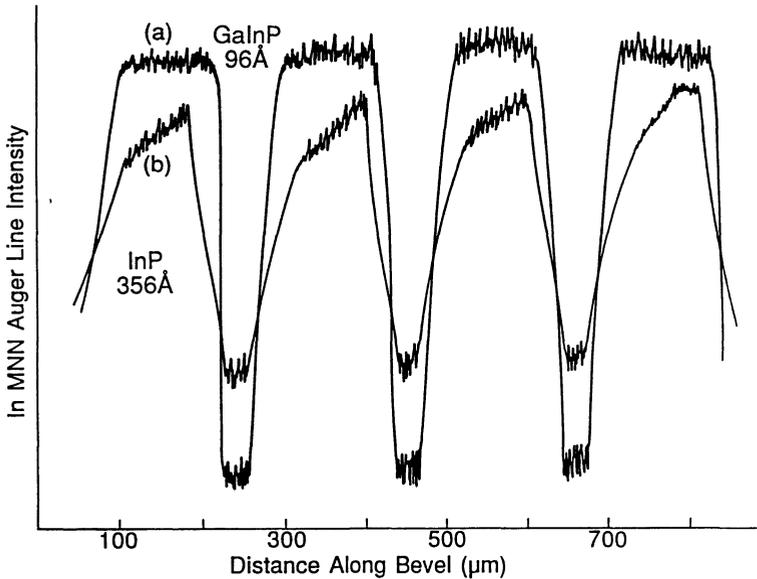


Fig. 6. — In line scans across ion beam bevelled section of GaInAs/InP superlattice: a) bevelled using 2 KeV Xe⁺ ions; b) the same bevel section after removing $\sim 500 \text{ \AA}$ of the surface using ArO₂/Cl CARIBE process.

very thin layers. A typical laser structure is shown in Figure 8 with the main area of interest for analysis being in the quantum well region and graded layers. The function of the composition graded layers is to provide a graded index for the confinement layers. The aim of the design being to produce a linear grade between the binary compound to whatever composition is required in the ternary or quaternary layer. The role for AES in the characterisation of these structures is quantification of the matrix elements in the layers and to measure the linearity of the graded layers. A bevel sputtered into a similar structure is shown in Figure 2. The compositional line scan across the region of interest is P, chosen for its superior signal to noise ratio and low energy (120 eV). It provides an example of bevel section application, quantification of the bevel excursion being made in discrete points along its length. Measurements made in this region of the device structure would normally be made before growth of the much thicker top layers to keep sputter damage at a minimum. As might be expected with such complex structures, AES is only one of the many analytical techniques required for full characterisation. Similar structures are also produced using AlGaAs and experiments carried out to determine the sputtering characteristics of this compound were aimed primarily at finding the optimum sputtering conditions for high resolution profiling [24]. The results revealed that not only is it necessary to find the optimum conditions for each compound, but that these conditions may vary with a particular compound depending on the ratio of elements it contains. An example of this effect is presented in Figures 9 and 10. Plots ΔZ vs. Z for two GaAlAs/GaAs superlattice structures with different Al contents are shown in Figure 9. Curve a) with the higher Al content was plotted from the data in Figure 10 and shows $\Delta Z/Z$ relationship normally associated with polycrystalline materials. Curve b), with half the Al content, follows a Z dependence obtained from amorphous oxides [25], with the plateau region extending up to Z values of 400 nm before surface roughening effects begin to dominate. The conclusion reached in this study was that the degrading resolution in Figure 10 a) is caused by enhanced atomic mixing brought about by the deeper implantation of the Al atom as

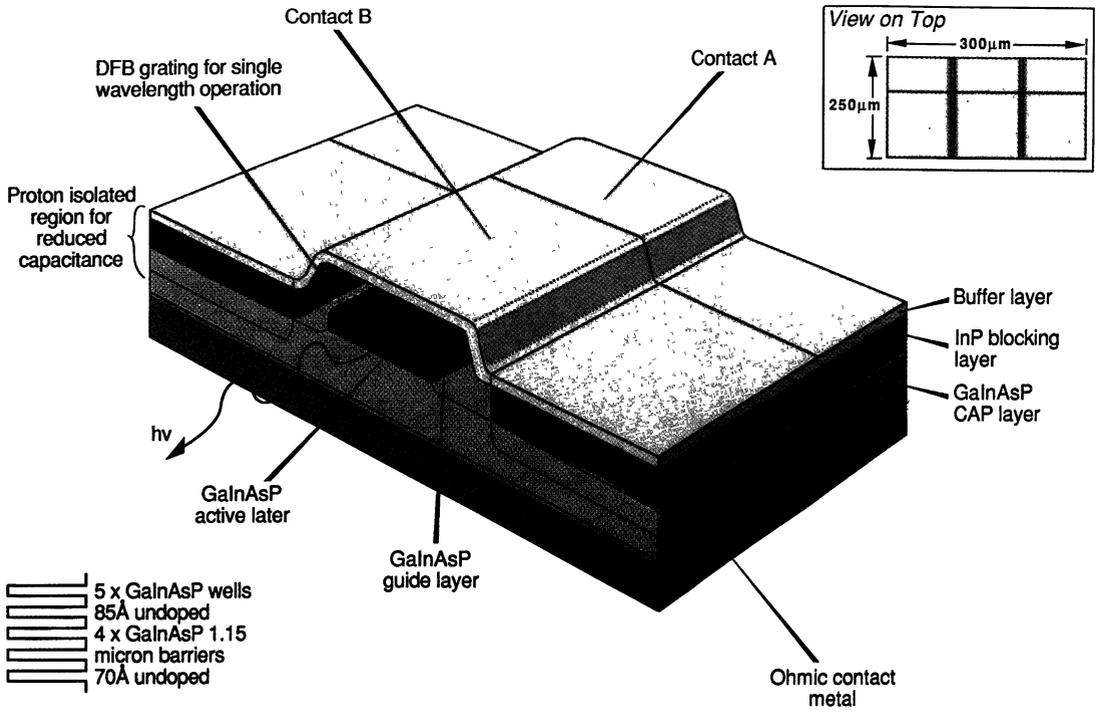


Fig. 7. — Schematic of laser device.

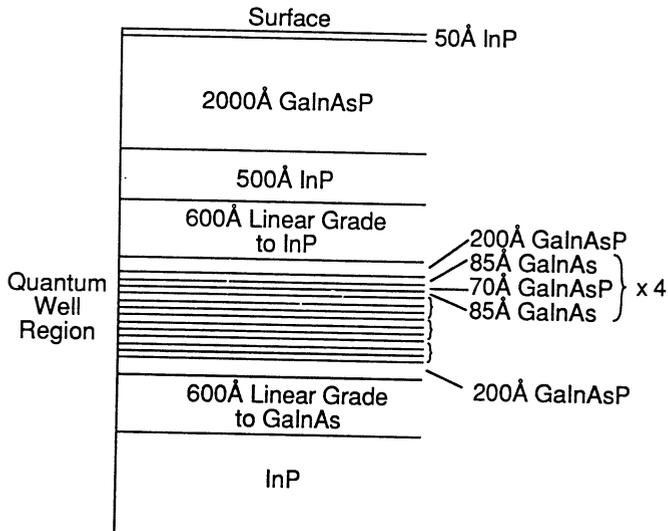


Fig. 8. — Schematic showing the semiconductor layer structure of a graded refractive index multiple quantum well laser.

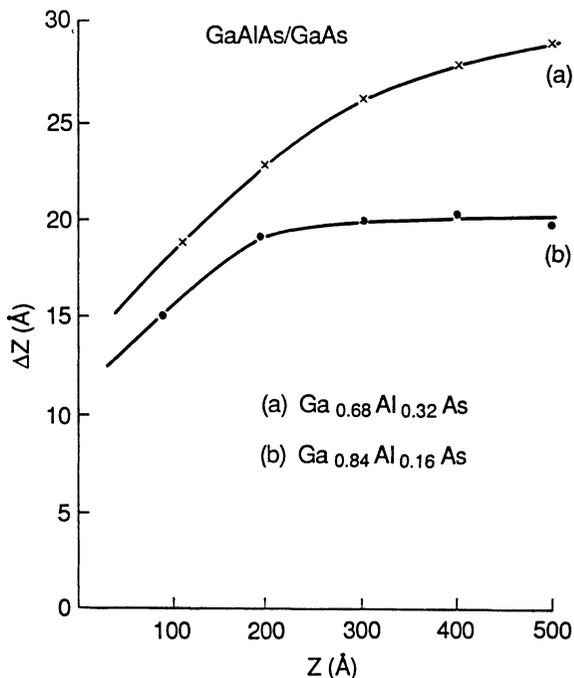


Fig. 9. — The depth resolution as a function of interface depth using 700 eV Xe⁺ ions incident at 50° from the surface normal for two different Al levels in AlGaAs/GaAs.

a consequence of its low mass.

An interesting demonstration of the combined efforts of transmission electron microscopy (TEM) and AES in solving problems associated with the growth of AlGaAs layers is shown in Figure 11. Routine thickness measurements of these layers occasionally reveals problems with the layers or at interfaces. In this example, the contrast variation revealed by TEM was subsequently revealed by AES to be instability in the Al content. The Auger profile in this figure shows the quantification of part of the layer. A good proportion of work carried out by AES in this industry interrelates with other analytical techniques in this way, either confirming a finding or providing extra information and can broaden the scope of an investigation considerably.

6. Quantitative Accuracy

While AES has become a widespread analytical technique in the semiconductor industry, its capacity for accurate quantitative analysis, particularly of compound semiconductor material has been the subject of much discussion [26, 27]. Few analytical techniques can tackle the quantitative analysis of these materials in such thin layers and complex structures. The predominant problem for Auger analysis relates to the necessity for sputter etching either to remove surface contamination, or in the process of producing an Auger profile. From the list of sputter induced artefacts in Table III, only preferential sputtering need concern us here. It is the effect which most seriously complicates the quantitative assessment of III-V materials.

It is essential that the sputtering behaviour of the specific material is studied before attempting its analysis. This can be done by recording the Auger peak ratios of the binary compounds, both vacuum cleaved and after significant sputtering for the peak ratios to stabilise [28]. Figure 12a

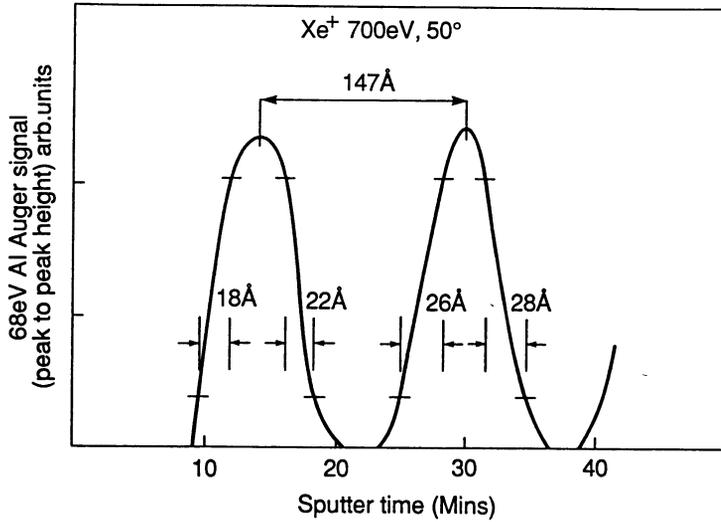
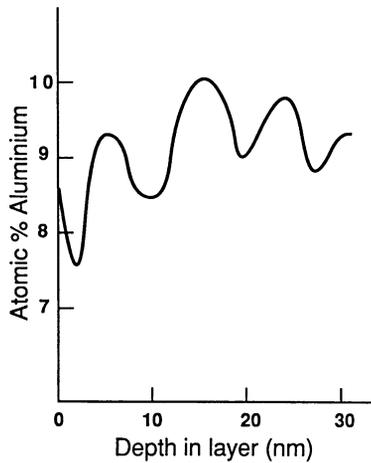
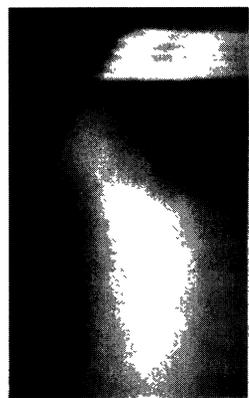


Fig. 10. — AES profile of the top 4 layers of a $\text{Ga}_{0.68}\text{Al}_{0.32}\text{As}/\text{GaAs}$ superlattice structure showing degrading interface resolution with increasing sputtered depth.

Analysis of Al in AlGaAs

CLEAVED EDGE TEM
Dark field g_{200} image

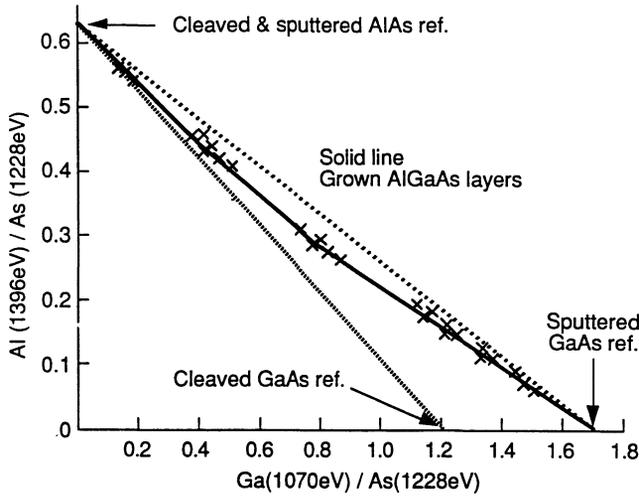
AUGER PROFILE



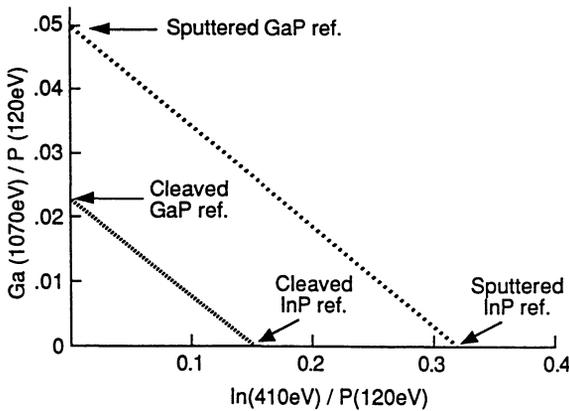
Brightness of the image
is proportional to the
Al content

Fig. 11. — a) cleaved edge TEM image of composition variation in AlGaAs layer; b) Auger profile showing extent of Al instability in AlGaAs layer.

shows the result of an exercise using GaAs and AlAs for preferential sputtering corrections in the analysis of the ternary AlGaAs. The figure shows that AlAs is not subject to preferential sputtering, whereas GaAs is. In addition, there does not appear to be a linear relationship between AlAs and GaAs. This becomes apparent when data is added to the plot from AlGaAs samples. Figure 12b is a repeat of this exercise for the ternary GaInP using GaP and InP, and shows that



(a)



(b)

Fig. 12. — a) plot of cleaved and sputtered Al/As vs Ga/As peak height ratios; solid line data obtained using peak height ratios from AlGaAs layers; b) plot of cleaved and sputtered Ga/P vs In/P peak height ratios. Sputter etch conditions 2 KeV, Xe+.

both GaP and InP are subject to preferential sputtering. In practice, because of the necessity for quantitative accuracy in the characterisation of these structures, a range of samples are produced specifically for calibration and checked by several analytical methods.

The III-V structures used as examples in this paper were all grown using metal organic vapour phase epitaxy (MOVPE). This is now a widespread growing method for semiconductor materials and capable of growing single crystal layers down to 20 Å thick. Figure 13 is the result of an exercise in correlating Auger analysis of MOVPE grown layers against the composition calculated using the growth conditions of the MOVPE reactor in which they are grown. The solid line in this figure is from a calculation using the molar fractions of the organics to determine the compositions in the vapour. A large part of the effort given to the analysis of III-V materials is aimed at constant

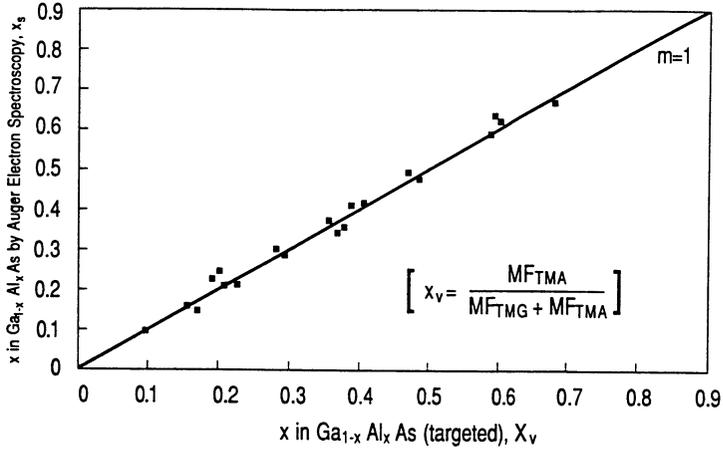


Fig. 13. — Plot showing correlation of Auger data from AlGaAs layers with that using a calculation based on the molar fractions of the organics, trimethyl Ga (TMG) and trimethyl Al (TMA) to determine the composition in the vapour; solid line.

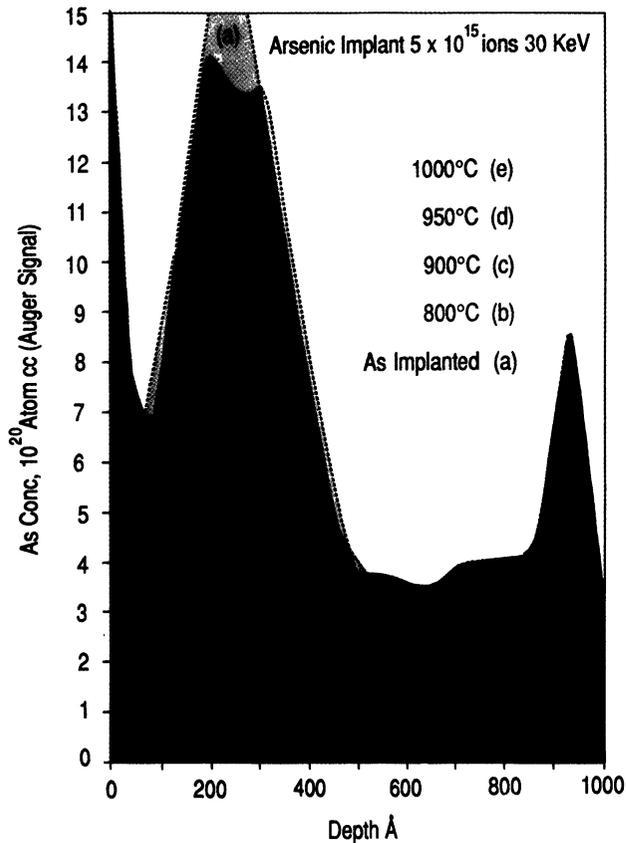


Fig. 14. — Auger profile of the depth distribution of arsenic in polysilicon layers after rapid thermal annealing at various temperatures.

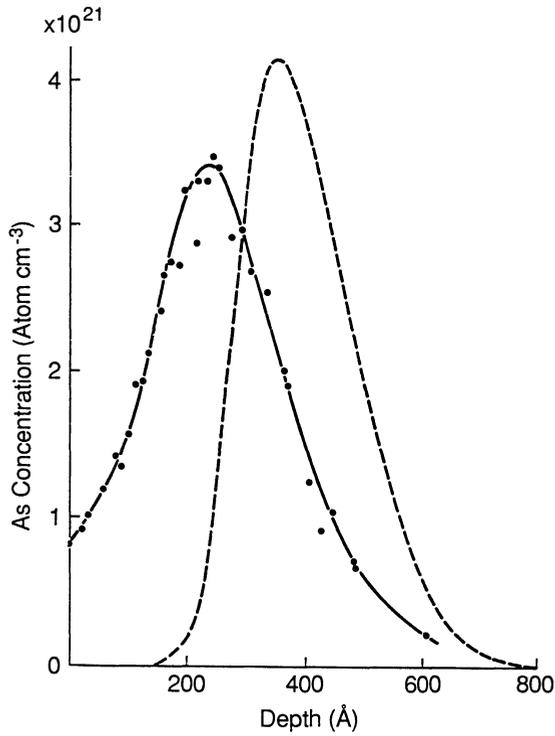


Fig. 15. — AES arsenic implant profile (40 KeV, 10^{16} atoms/CC). Dotted curve = SUPREM simulation.

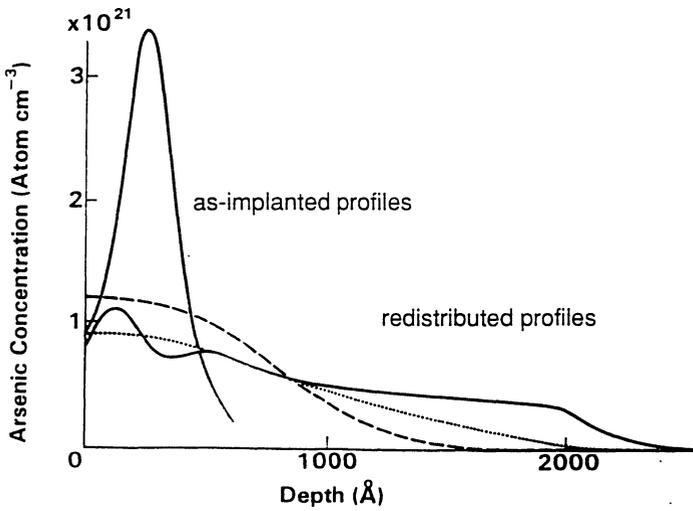


Fig. 16. — AES arsenic implant profiles showing redistribution of arsenic by transient anneal : dotted lines are SUPREM simulations using different default values.

Polysilicon Emitter Structure

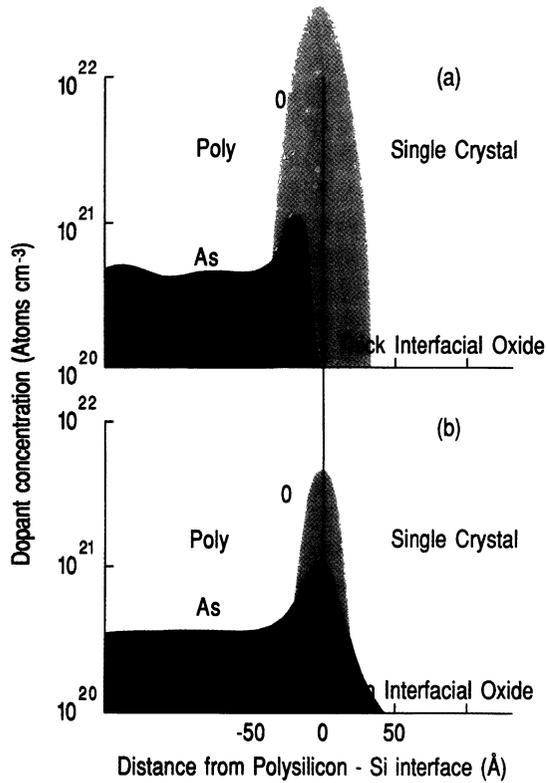


Fig. 17. — AES dopant concentration profiles through the polysilicon/single crystal Si interface region of a poly emitter transistor structure for a) 57 Å and b) 12 Å interfacial oxides : polysilicon top layer 1000 Å thick.

calibrations of the MOVPE reactors and is an important role, not only AES but all the other relevant techniques.

7. Silicon Technology and Process Modelling

Very large scale integration (VLSI) technology where high dopant concentrations are ion implanted into shallow layer structures is an area where AES has been demonstrated to make a valuable contribution [29]. Although the profiling of dopants in semiconductor structures is normally considered to be outside the detection limits of AES, the high dopant concentrations used in VLSI structures has made it possible for AES to provide a valuable complement to secondary ion mass spectroscopy (SIMS) analysis. The advantage of AES in this situation is the absence of the matrix effects SIMS is sensitive to. This is of great importance at surfaces and interfaces. An example of AES dopant profiles in Si is shown in Figure 14, where five samples are superimposed and show the redistribution of As as a function of annealing temperature. To extend the detec-

Buried Oxide Thickness Measurement

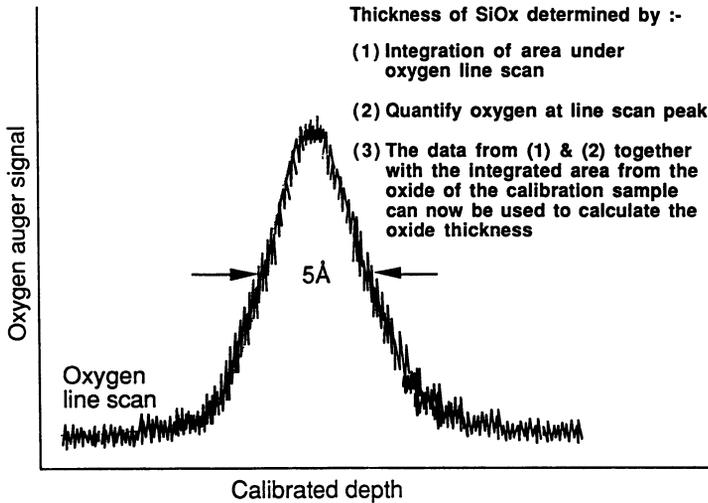


Fig. 18. — Ion beam bevel section of a 5 Å oxide at a Polysilicon/Si interface.

tion limits of AES to doping levels in the mid 10^{19} cm^3 region is not a trivial matter and requires optimisation of all the spectrometer operating conditions to achieve the necessary signal to noise levels. The main purpose of the examples of AES profiling of dopants in silicon presented in this paper has been to provide input into process modelling programmes [30]. The aim of process modelling is to relate quantitatively the final device structure to the relevant variables of the fabrication process. These programmes have become an integral part of the design of the process to produce the desired electrical properties of the devices. Access to a facility that can simulate the cumulative effects of the large number of sequential steps in integrated circuit processing is of inestimable value in their design.

Developing the required physical theories and mathematical models for process modelling requires accurate experimental data, both as input to the model and as the ultimate check of the correspondence between predicted and actual device structures. Towards this end, Auger profiling has been used to establish implanted dopant distributions accurately at the peak region of the implant, and at the substrate interface before and after anneal cycles. One of the early efforts at simulation is shown in Figure 15, together with the true distributions as revealed by Auger profiling. The simulation showing considerable error in terms of the depth, width and peak intensity of the implant. Calibration of the Auger data from implanted samples is by integration of the implant dose which is known accurately.

After ion implantation, the dopant in a VLSI structure will require a heat treatment to put it into active sites and to redistribute it as required for optimum device performance. The transient anneal requirements for VLSI structures are concerned with the redistribution of dopant within the constraints of the generally reduced device dimensions. Figure 16 contains Auger profiles before and after transient anneal, together with two attempts at simulations based on earlier methods of annealing. The capability to model redistributions occurring at each process stage accurately is essential if the final device structure is to be adequately represented. The process modelling programmes are therefore critically dependent on high resolution distortion free profiles.

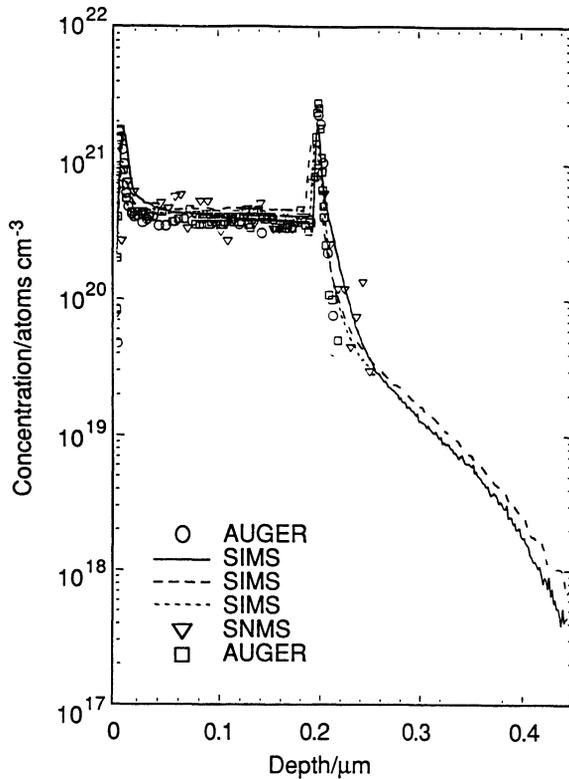


Fig. 19. — Depth profiles of 2000 Å polysilicon/silicon sample implanted with arsenic -10^{16} atom cm^{-2} 50 KeV, and furnace annealed at 900 °C for 30 min.

A further demonstration of the need for high resolution profiling are the Auger profiles in Figure 17. Of particular interest here is the effect of thin SiO_2 layers at the interface between polycrystalline Si and the single crystal Si substrate. This oxide acts as a barrier to the diffusion of As into the Si substrate during anneal cycles. This experiment clearly shows the effectiveness of the 57 Å oxide in preventing As diffusion into the substrate.

8. Subnanometer Buried Oxides

In modern bipolar devices, a polysilicon layer serves as the diffusion source for the emitter and as the emitter contact. The crystallographic nature of the polysilicon and the way in which it acts, both as diffusion source and as a contact, is dependent upon the thickness and integrity of the interfacial oxide between the polysilicon and the underlying single crystal Si. Measuring the thickness and integrity of these interfacial oxides before and after various thermal treatments is carried out by AES and TEM [31]. Under certain annealing conditions, the oxide breaks up and only cross-section TEM is capable of detecting this effect. The thickness of the oxide can be measured using AES in conjunction with the 'ion beam bevel section' discussed earlier. Figure 18 shows an Auger line scan for oxygen across a 5 Å buried oxide from a bevelled section which had been post sputtered at low energy and grazing incidence to improve resolution. The 5 Å oxide is increased to 25 μm on the bevel and the line scan produced by scanning with an electron beam of

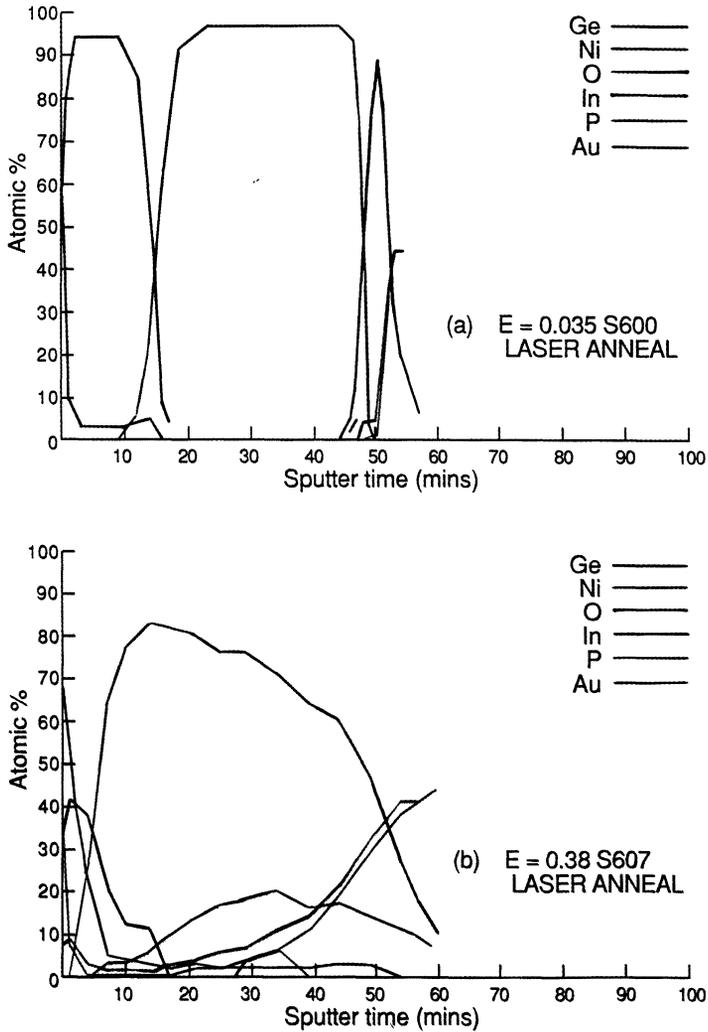


Fig. 20. — AES profile of laser annealed NiGeAu contacts on InP at two different laser energy densities.

$1 \mu\text{m}$ diameter. The thickness of the oxide can now be determined by:

- recording the Auger line scan for oxygen.
- quantifying the oxygen concentration at its peak
- integrating the area under the oxygen line scan.
- using the integrated area of the calibration sample to calculate the thickness of the oxide.
The accuracy of this method is dependent on the availability of suitable reference samples.

9. Multiple Technique Analysis

Collaborative programmes of analytical work with the application of several techniques to the same sample are of immense value, not only in giving greater confidence in the accuracy of analysis, but by providing as it does a much more detailed picture of the chemistry and morphology of the sample. An example from a collaborative venture is shown in Figure 19 and contains data from SIMS secondary neutral mass spectrometry (SNMS) and AES.

The project presented an opportunity to show how the strength of each technique can be revealed by bringing together data obtained from the same samples (dopant implants in Si). This enabled a detailed analysis of the overlap between techniques of different sensitivity, methodology and resolution limitations. Auger profiling for example gave quantifiable data in the high concentration regions, in particular the near surface and interface accumulations. The agreement in depth calibration between techniques was < 5%. The concentration was in good agreement (< 15%) where the dopant variation was slow. The larger discrepancy in areas of rapid concentration change are attributed to variations in atomic mixing resulting from the different sputtering beam energies used in the various techniques. The most important result from this exercise was the excellent agreement achieved between techniques based on quite different physical mechanisms and the valuable data it provided for Si technology.

10. Metal Semiconductor Contacts

Another area where Auger profiling is of particular value is in contact behaviour. The electrical behaviour of ohmic and Schottky barrier contacts to III-V materials is dominated by the compositional and morphological features at the interface. Ohmic contacts for example are usually multi-metal layered structures and require various annealing cycles to activate them. The Auger profiling can provide information concerning metallurgical reactions occurring at interfaces and grain boundary and bulk inter-diffusion. The normal procedure for contact annealing is the 'rapid thermal anneal' using a radiant heat source and cycle times as brief as one second. Experiments using laser annealing [32] have been tried which have anneal times of 25 ns. The two profiles in Figure 20 of a NiGeAu contact on InP were selected from a series of profiles covering a wide range of gradually increasing laser energy. The energy provided by the Q-switched ruby laser penetrates less, enabling higher annealing temperatures to be reached.

The two profiles selected are from the beginning and middle of the laser energy range used and reveal the enormous changes that have occurred during the anneal. Interpretation of such profiles is far from straightforward, requiring as it does a detailed knowledge of the metallurgical reactions and diffusion mechanisms involved, together with an awareness of the sputter induced artefacts which have almost certainly added to the complexity of the analysis.

The Schottky barrier contact is a junction between a metal and semiconductor which sets up a barrier potential and has rectifying properties similar to a p-n junction. Chemical bonding at the metal-semiconductor interface is the determining factor in barrier formation and has been the subject of many AES studies [33, 34]. It has been demonstrated by AES for example that Al deposited on InP can result in either an ohmic contact or Schottky barrier depending on surface treatment prior to Al deposition [35]. Metallisation also includes the use of fine Al rails as conducting paths. The small dimensions mean that electromigration of the Al can be a problem and to reduce this effect a small percentage of Cu is added to the Al. The subsequent migration of Cu to the substrate interface on annealing is revealed by the Auger profile in Figure 21. Also included in Figure 21 is the result of a cross-section TEM analysis. This outline drawing, taken from the TEM photograph for clarity, reveals that although the Auger profile is broadly correct, important detail is missing. Cu has in fact migrated to grain boundaries to form CuAl_3 precipitates, most

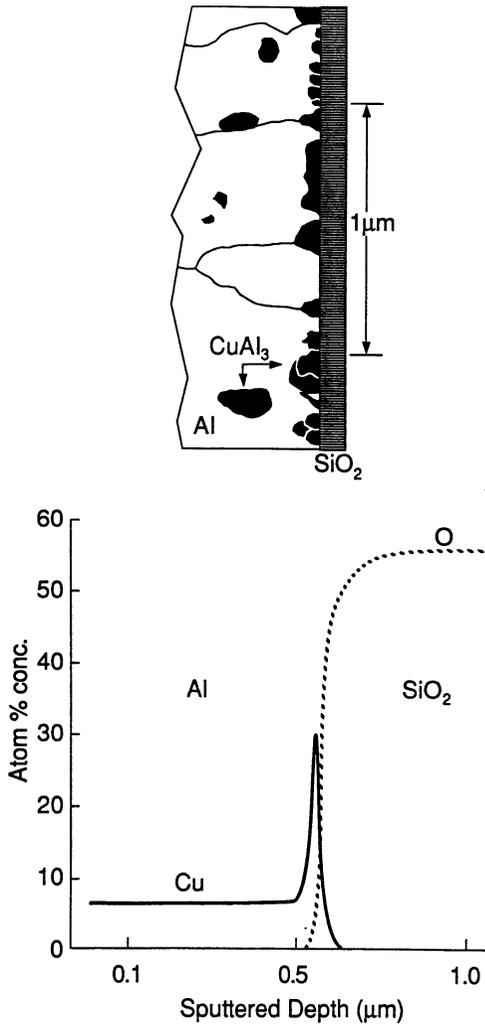


Fig. 21. — AES profile from Al film with 5% Cu deposited on SiO_2 showing migration of Cu to the interface after heat treatment, together with the structural information provided by cross-section TEM showing the formation of CuAl_3 precipitates.

of which are at the interface with the substrate. This example has been included to show the important information that can be missed in analysis. A 2D profile using high resolution scanning Auger microprobe (SAM) would have detected the precipitation, but before committing the time required for such a profile, it would have been necessary to suspect their existence.

11. Closing Remarks

It is impossible to give anything other than a sample of the wide range of AES analysis in this industry. As might be expected, much of the application is of a repetitive nature and is largely concerned with the continuity of quality at the various processing stages.

The requirements of industry are changing, with greater emphasis on quality assessment and less on research topics. Limited budgets for new equipment has also led to a re-assessment of how best to combine analytical techniques to give a more cost-effective service. In the past this was considered to compromise optimum performance, but improvements in instrument design have mitigated this objection to some extent.

In general terms, the electronics industry requires a fast turnaround in analysis and the role for AES is to a large extent dependent on being able to provide such a service. Methods of improving the turnaround time for AES would include:

- increasing the rate of data acquisition by improved analyser design, multi-channel system, etc. for increased collection efficiency.
- developing improved high current - low energy ion guns for profiling.
- developing small diameter electron beam probes - around 100 Å would allow vacuum cleaved analysis of thin layers, thereby avoiding the necessity for sputter etching.
- improving software for data handling and instrument control based on the 'expert system' concept.

The question of quantitative accuracy and its degradation by sputter induced artefacts has been discussed in this paper and is still of some concern for the more susceptible materials. Considerable progress has certainly been made in the reduction and understanding for these artefacts [36, 37], but the diversity of these effects is such that future prospects for accurate qualification of AES data is, for many materials, dependent on continuing progress from investigations in this field.

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References

- [1] El Gomati M.M., Prutton M., Lamb B., Tuppen C.G., *Surf. Interface Anal.* **11** (1988) 251.
- [2] Cazaux J., *Surf. Interface Anal.* **14** (1989) 354.
- [3] Cazaux J., *J. Microsc.* **145**, Pt. 3 (1987) 257.
- [4] Seah M.P., Tosa M., *Surf. Interface Anal.* **18** (1992) 240.
- [5] Prutton M., El Gomati M.M., Kenny P.G., *J. Electron. Spectrosc. Rel. Phen.* **52** (1990) 197.
- [6] Powell C.J., *Surf. Interface Anal.* **17** (1991) 308.
- [7] Werner W.S.M., *Surf. Interface Anal.* **18** (1992) 217.
- [8] Tanuma S., Powell C.J., Penn D.R., *Surf. Interface Anal.* **11** (1988) 577.
- [9] Prutton M. *et al.*, *Surf. Interface Anal.* **17** (1991) 71.
- [10] Holloway P.H., Bhattacharga R.S., *J. Vac. Sci. Technol.* **20** (3), (1982) 444.
- [11] Carter G., Nobes M.J., Whitton J.L., *Appl. Phys. A.* **38** (1985) 77.
- [12] Carter G., Gras-Marti A., Nobes M.J., *Radiat. Effects* **62** (1982) 119.
- [13] Pamler W., Wangemann K., *Surf. Interface Anal.* **18** (1992) 52.

- [14] Seah M.P., Hunt C.P., *Surf. Interface Anal.* **5** (1983) 33.
- [15] Hofmann S., *J. Vac. Soc. Jpn.* **33** (1990) 721.
- [16] Auciello O., *J. Vac. Sci. Technol.* **19** (1981) 841.
- [17] Peacock D.C., *Vacuum* **33** (1983) 601.
- [18] Erikson L.P., Phillips B.F., *J. Vac. Sci. Technol.* **B1** (1983) 158.
- [19] Walls J.M., Hall D.D., Sykes D.E., *Surf. Interface Anal.* **1** (1979) 204.
- [20] Lee C., Seah M.P., *Thin Solid Films* **75** (1981) 67.
- [21] Bresse J.F., *Scanning Electron Microsc.* **4** (1985) 1465.
- [22] Skinner D.K., *Surf. Interface Anal.* **14** (1989) 567.
- [23] Williams P.J., Webb A.P., Goodridge I.H., Carter A.C., *Electron. Lett.* **22** (1986) 472.
- [24] Skinner D.K., Hill C., Jones M.W., MRS Symp. Proc., 48, W. Katz, P. Williams Eds. (San Francisco, U.S.A., 1985) 149.
- [25] Fine J., Navinsek B., Davarya F., Andreadis T.D., *J. Vac. Sci. Technol.* **20** (1982) 449.
- [26] Jardin C., Roberts D., Achard B., Gruzuya B., Pariset C., *Surf. Interface Anal.* **10** (1987) 301.
- [27] Malherbe J.B., Bernard W.O., Strydom Le. R., Louw C.W., *Surf. Interface Anal.* **18** (1992) 491.
- [28] Arthur J.R., Le Port J.J., *J. Vac. Sci. Technol.* **14** (1977) 979.
- [29] Hill C., Butler A.L., Inst. Phys. Conf. Ser., 69, ESSDERC/SSSDT (Canterbury, September, 1983) 161.
- [30] Hill C., Jones S.K., *Mat. Res. Soc. Symp. Proc. Col.* **182** (1990) 129.
- [31] Augustus P.D., Skinner D.K., Goulding M.R., Nigrin S., Beanland R., Inst. Phys. Conf. Ser. 134 (Oxford, April, 1993) 215.
- [32] Warwick University, Project GR/H 36613 IED/2/1540, Final Report to SERC (1994).
- [33] Topham P.J., Skinner D.K., Sealy B.J., Inst. Phys. Conf. Ser. 67 (Oxford, March, 1983) 183.
- [34] Skinner D.K., *J. Electronic Mat.* **9** (1980) 67.
- [35] Rhoderick E.H., *IEE Proc.* **129** Pt. 1, No. 1 (February, 1982) 1.
- [36] Hofmann S., *J. Vac. Sci. Technol.* **A9** (1991) 1466.
- [37] Carter G., Katardkiev I.V., Nobes M.J., *Surf. Interface Anal.* **14** (1989) 194.